**Department of Electronics and Communication Engineering**

**Question Bank for UNIT - 1**

**Name of Faculty member: Dr.S.Shiyamala Year /Sem : II/III**

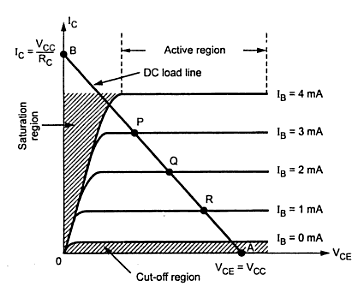
**1. What is Bias? (or) What is the need for biasing? (or)**

**write the significance of biasing (or) what is the need for biasing**

**(May’13)(Nov’12) (Nov’11) (Nov’08)**

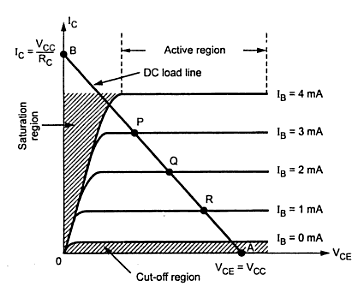
To fix the Q – point in the middle of the active region we go for Biasing. The proper flow of zero signal collector current and the maintenance of proper collector emitter voltage during the passage of signal is known as transistor biasing.

When a transistor is biased properly, it works efficiently and produces no distortion in the output signal and thus operating point can be maintained stable.



**2. What is the meant by operating point Q? (or) Enumerate the concept of Q point (or) Define quiescent point (Nov’13)(May’12)  (Nov’11)(Apr’08)**

The zero signal values of Ic & Vce are known as operating point. It is also called so because the variations of Ic and Vce take place about this point, when the signal is applied.



**3. What are the factors that affect the stabilization of collector current (May’12)**

The following are the factors that affect the stability of the operating point,

a. Transistor current gain factor - Change of hfe/β due to replacement of transistors.

b. Thermal variations - ICO, VBE, βdc

**4. What is Thermal runaway? (Nov’06)(May’14).**

Increase in collector current increase the power dissipation at the collector junction. This will increase the temperature and hence collector current increases.

This process is cumulative. This **excess heat** produced at the collector to base junction may burn and **destroy the transistor**. This situation is called **thermal runaway**

**5. Write the conditions of thermal stability (May ‘13)(Nov’07)**

The rate at which heat is released at the collector junction must not exceed rate at which heat can be dissipated under steady state condition to prevent thermal runaway.

**6. Define stability factor ‘S’? (Nov’12) (Nov’09)(May’12)(Apr’09)**

The stability factor is defined as the rate of change of collector current Ic with respect to the reverse saturation collector current Ico, keeping ‘Vbe’ and ‘β’ constant.



**7. Derive the stability factor S for a fixed bias circuit. (Nov’10)**

General form for stability factor is



The stability factor for the fixed bias circuit is,

S = 1+ β [because for fixed bias = 0]

**8. What do you understand by DC & AC load line? (Nov’12)**

DC Load Line :

It is the line on the output characteristics of a transistor circuit which gives the values of Ic & Vce corresponding to zero signal (or) DC Conditions.

AC Load Line :

This is the line on the output characteristics of a transistor circuit which gives the values of Ic & Vce when signal is applied.

**9. What is the drawback of collector to base bias? (May’06)**

a. The collector current is high.

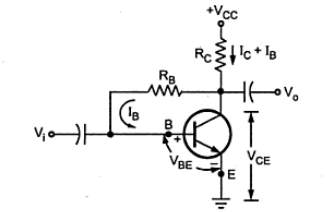
b. If AC signal voltage gain feedback into the resistor Re, it will reduce the gain of the amplifier.

**10. Why BJT needs temperature compensation against VBE changes (May’06)**

Because when VBE changes due to temperature then IB changes so collector current

varies. So temperature compensation is required.

**11. Draw the circuit of collector to base bias feedback biasing circuit (Nov’06)**

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**12. Is it necessary to stabilize the operating point of transistor why (Nov’05)**

**Yes , stabilizing the Q point is necessary . otherwise positive peak clips or negative peak clips may happened if Q point shifted nearer to saturation or cut off region**

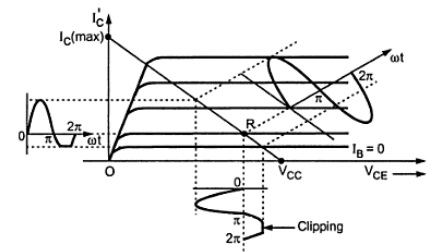
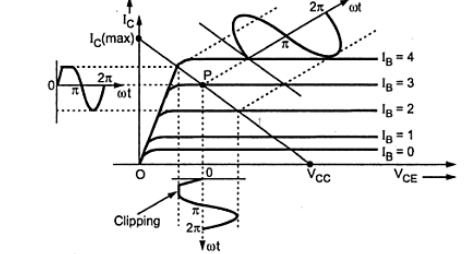
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Fig : (a) Q- nearer to saturation – positive clip (b) Q – nearer to cutoff – negative clip

**13. What is meant by compensation technique (Apr’04)**

Compensation techniques: This refers to the use of temperature sensitive devices such as thermistors, sensistors , diodes etc. They provide compensating voltages &currents to maintain operating point constant.

**14. What are the advantages of self bias circuits? Why voltage divider bias is commonly used in amplifier circuit? (or) What are the advantages of self bias over other types of biasing (or) which is the most suitable biasing circuit why? (Nov’12)**

**(May’12)(Nov’11) (Nov’09)**

Stability factor S for voltage divider bias is less as compare to other biasing circuits. So this circuit is more stable and hence it is more commonly used.

**15. What is the condition for thermal stability?(Nov’13)(May’13)(Nov’07)**

The rate at which heat is released at the collector junction must not exceed rate at which heat can be dissipated under steady state condition to prevent thermal runaway.

**16. Draw the fixed and self bias circuits (Nov’08)**

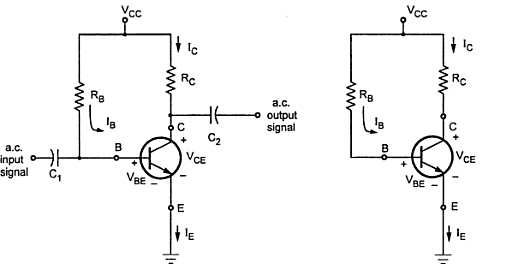
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Fig : Fixed bias circuit Fig : Dc equivalent of fixed bias

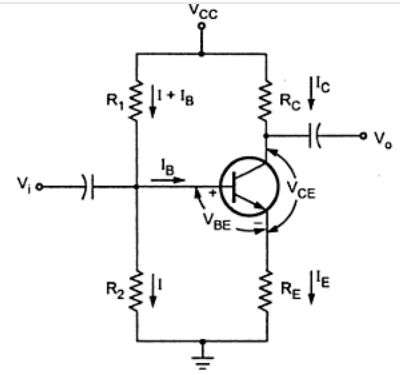


Fig : Self bias

**17. Why capacitor coupling used to connect a signal source to an amplifier? (Nov’07)**

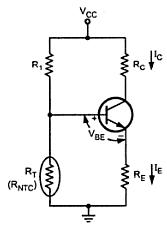
Coupling capacitor blocks DC voltage but freely allows AC signal as well as reduce loading effect between source and circuit results in which biasing conditions are maintained constant.

**Part B**

1. **What is the bias compensation using thermistor (Apr’08)**

**(or)**

**How can collector current be stabilized with respect to ISC variations? (Nov’10)**

1. **Thermistor Compensation**

(i)Thermistor has a negative temperature coefficient (NTC), its resistance decreases exponentially with increasing temperature.

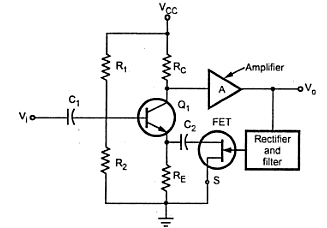
(ii)Here R2 is replaced by thermistor RT in self bias circuit.

(iii)With increase in temperature, RTdecreases.

(iv)This voltage drop is nothing but the voltage at the base with respect to ground. Hence VBE decreases which reduces IB. This behavior will tend to offset the increase in collector current with temperature.

**2. Explain the use of JFET as a variable voltage resister (Nov’06)**

**The use of JFET as a variable voltage resister is AGC (automatic gain control) in multi stage amplifier.**

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**3.Explain the methods of stabilizing the Q point. (8)**

**(May’12)(Nov’12)(May’13)(Nov’09)**

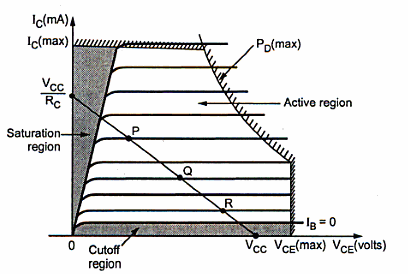
**(or)**

**Discuss the various techniques of stabilization of Q-point in a transistor (16)(May’12)**

* Biasing circuit should be designed to fix the operating point or Q point at the centre of the active region.
* Designing the biasing circuit to stabilize the Q point is known as **bias stability.** Two important factors are (i) temperature (ii) transistor current gain.
* Stabilization techniques refer to the use of resistive biasing circuits which allow IB to vary so as to keep IC relatively constant with variations in ICO, β, and VBE.

1. **Temperature**
2. **ICO**

* The flow of current in the circuit produces heat at the junction.
* This heat increases the temperature at the junction.
* Minority carriers are temperature dependent. So ICO  increases.
* Due to increase in ICO  , collector current IC also increases..
* It raises the temperature at the collector junction.
* The excessive increase in collector current shift the operating point into the saturation region.
* Increase in collector current increase the power dissipation at the collector junction. This will increase the temperature and hence collector current increases.
* This process is cumulative. This excess heat produced at the collector to base junction may burn and destroy the transistor. This situation is called **thermal runaway**



1. **VBE (Base to emitter votage)**

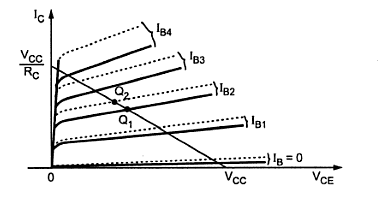
* Base current depends on VBE , Collector current depends on IB and VBE.
* Collector current changes with temperature due to change in VBE..
* The change in collector current change the operating point.

1. **βdc**

**IC  = β IB**

‘β’ also depends on temperature. Change in collector current change the ‘β’ value. Change in ‘β. Change then operating point.

1. **Transistor current gain hfe/β**



* The biasing circuit is designed according to the required ‘β’ value. But due to the change in ‘β’ from unit to unit, the operating point may shift.

**4. Explain with neat diagram of fixed bias circuit (8)( NOV’11)**

**(or)**

**With schematic diagram explain the working of a fixed bias circuit using JFET (NOV’09)**

**(or)**

**Explain the circuit of gate bias for providing stabilization of JFET (8)(Nov’13)**

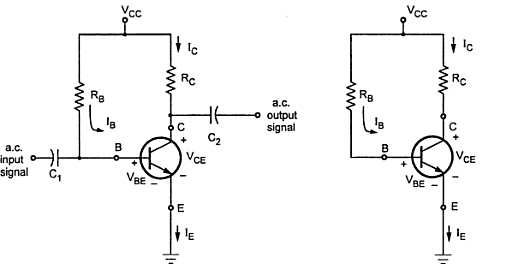
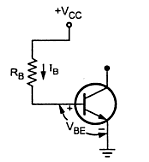


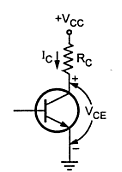
Fig : Fixed bias circuit Fig : Dc equivalent of fixed bias

1. **Circuit Analysis**
2. **Base circuit**

It is the simplest DC bias configuration



**(ii) Collector Circuit**



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**5.Draw a voltage divider bias BJT network and derive all the stability factors S, S’ and S’’.**

**(or)**

**Derive equations for the three stability factors**

**(or)**

**Draw the circuit of a voltage divider bias ircuit. Explain its operation and discuss how it stabilizes against VBE  changes**

**(or)**

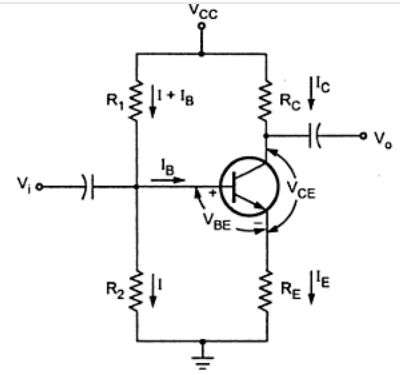
**With neat circuit diagram and needed expressions, explain the working principal of self bias of transistor.**

**(or)**

**Determine the stability factor for variations of ICO, VBE and β of a self bias circuit used in BJT amplifiers. (16)**

**(Nov’07)(May’07)(May’06)(May’12)(May’13)(Nov’13)(May’14)**

**Voltage Divider Bias / Self Bias Circuit**



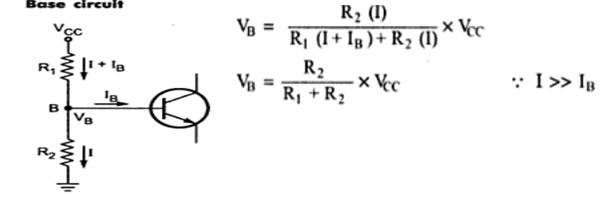
1. R1 , R2 – Potential divider

2. If Ic increases , IE also increases it reduces the voltage drop across base and emitter (VBE)

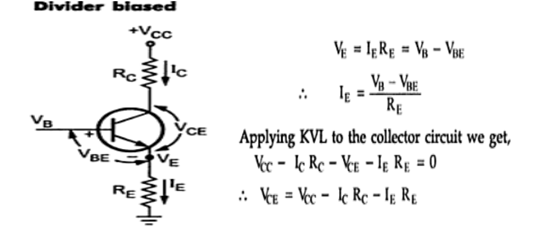
3. due to reduction in VBE  , base current and collector current get reduced.

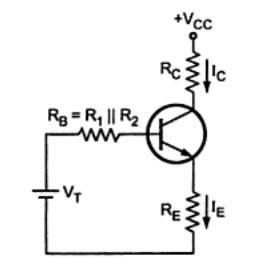
4. Negative feedback exists in the emitter bias circuit.

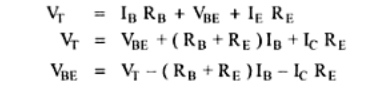
**Circuit Analysis**



**Collector circuit**

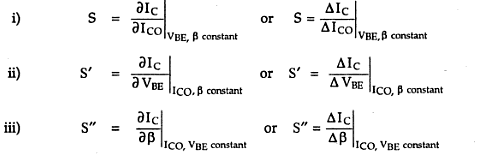
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**Simplified circuit of Voltage divider bias**

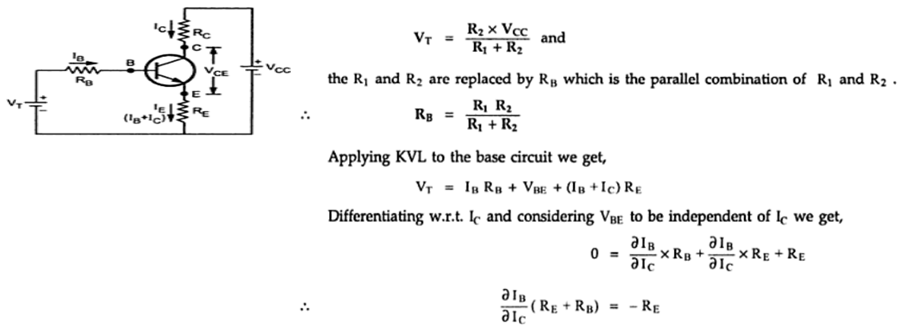


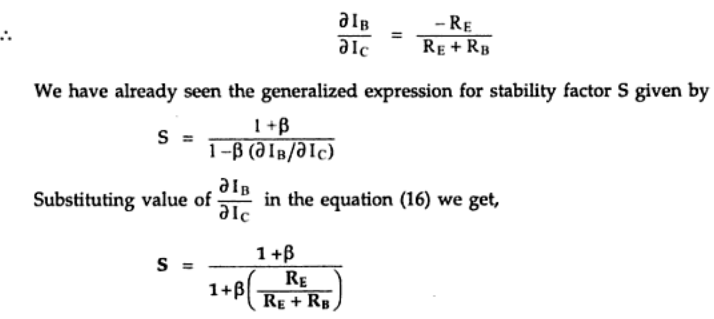
**Stability Factor**

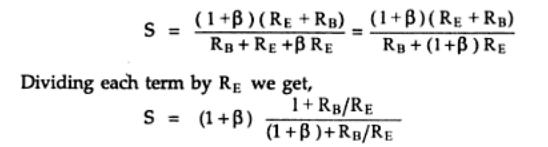
* **Ideally stability factor should be perfectly zero to keep operating point stable**
* **Practically stability factor should have the value as minimum as possible.**

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**Stability fact of S for voltage divider bias / Self Bias circuit**

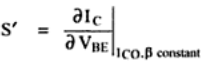


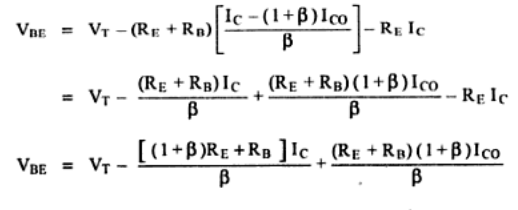
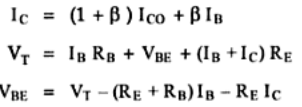


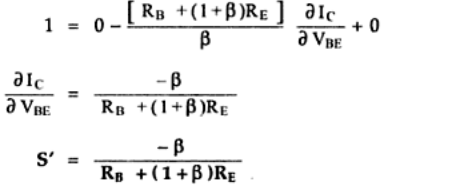


Advantage of Self bias: Stability factor S for voltage divider bias is less as compare to other biasing circuits. So this circuit is more stable and hence it is more commonly used.

**Stability factor S’**

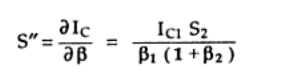






**Stability factor S’’**

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Advantages of self bias

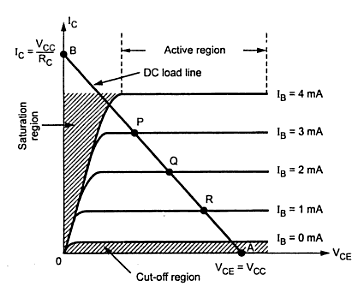
Stability factor S for voltage divider bias is less as compare to other biasing circuits. So this circuit is more stable and hence it is more commonly used.

**6. Why biasing is necessary in BJT amplifier and explain the concept of DC load line with neat diagram.(8) (Nov’07)**

**(or)**

**What is stability? What is the need for load line and quiescent point calculation (May’14) (6)**

* The proper flow of zero signal collector current and the maintenance of proper collector emitter voltage during the passage of signal is known as transistor biasing.
* When a transistor is biased properly, it works efficiently and produces no distortion in the output signal and thus operating point can be maintained stable.
* The operating point of a transistor is kept fixed usually at the center of the active region in order that the input signal is well amplified. If the point is fixed in the saturation region or the cut off region the positive and negative half cycle gets clipped off respectively.

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* The line drawn between A and B is called DC load line.
* The dc load line is a plot of IC vs VCE .
* Knowing any one of IC, IB or VCE it is easy to determine the other two from the load line. The intersection of curves of different values of IB  with dc load line gives different operating points.
* The operating point of a transistor is kept fixed usually at the center of the active region in order that the input signal is well amplified.
* If the point is fixed in the saturation region or the cut off region the positive and negative half cycle gets clipped off respectively.

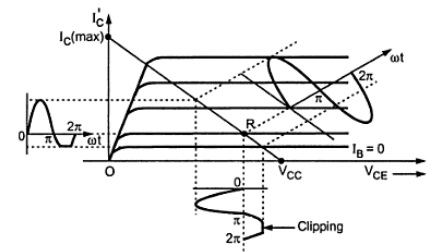
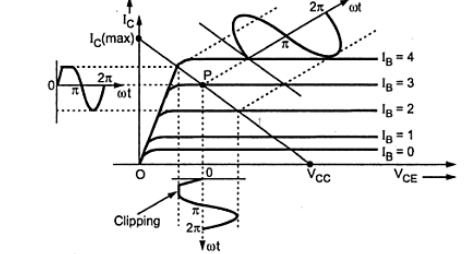
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Fig : (a) Q- nearer to saturation – positive clip (b) Q – nearer to cutoff – negative clip

**7. Discuss in detail about the various bias compensation techniques.**

**(or)**

**Write short notes on thermistor and sensistor compensations**

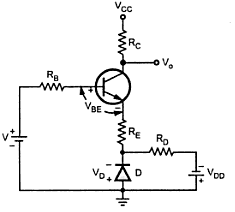
**(or)**

**Briefly describe about any two bias compensation techniques of BJT**

**(May’14)(May’12) (Nov’12) (June ‘13) (Nov’11)**

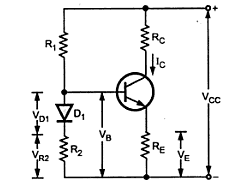
1. **Diode compensation technique**

**(i)Compensation for VBE**

**(a)Diode in emitter circuit**

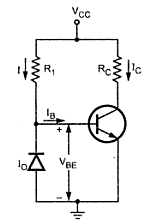
* Separate supply voltage VDD is used to keep the diode in forward bias.
* When VBE changes by əVBE with change in temperature, VD changes by ə VD, the change tend to cancel each other
* VD tracks VBE with respect to temperature, IC will be insensitive to variation in VBE.

**(b) Diode in voltage divider bias**



(i)Biasing is provided by R1, R2 and RE..

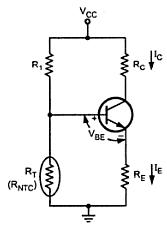
(ii)The changes in VBE due to temperature are compensated by changes in the diode voltage which keeps IC stable at Q point.

** (ii) Compensation for ICO**

(i)The diode is kept in reverse bias condition.

(ii)During reverse bias condition, leakage current only passes through diode.

(iii)Leakage current of the diode will increase with temperature at the same rate as the collector leakage current ICO

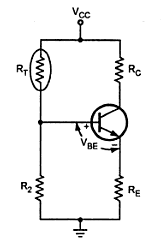
1. **Thermistor Compensation**

(i)Thermistor has a negative temperature coefficient (NTC), its resistance decreases exponentially with increasing temperature.

(ii)Here R2 is replaced by thermistor RT in self bias circuit.

(iii)With increase in temperature, RTdecreases.

(iv)This voltage drop is nothing but the voltage at the base with respect to ground. Hence VBE decreases which reduces IB. This behavior will tend to offset the increase in collector current with temperature.

1. **Sensistor Compensation**

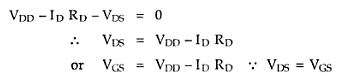
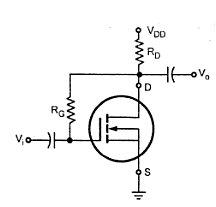
(i)Sensistor has a positive temperature coefficient (PTC), its resistance decreases exponentially with decreasing temperature.

(ii)Here R1 is replaced by sensistor. As temperature increases, RT increases which decreases the current flowing through it.

(iii)Hence current through R2 get reduced, which reduces voltage drop across it. So VBE reduces which decreases IB .

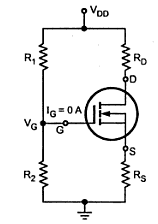
**8. Draw two biasing circuits for an enhancement type MOSFET (6) (Nov’12) (Nov’13)**

1. **Feedback bias circuit**



* For the DC analysis ,replace coupling capacitor by open circuits

1. **Voltage Divider bias**

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(Note : derivation everything same as biasing using transistor)

**9.Discuss in detail about any of the FET biasing techniques (8)     (Nov‘11)(May’07)(May’06)**

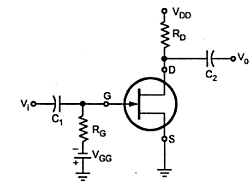
**(or)**

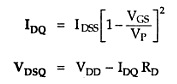
**With schematic diagram explain the working of a fixed bias circuit using JFET (NOV’09)**

**(or)**

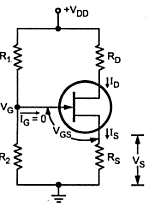
**Explain the circuit of gate bias for providing stabilization of JFET(8)(Nov’13)**

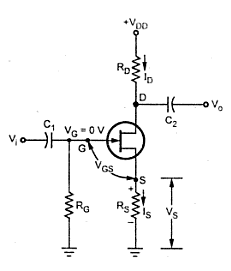
1. **Fixed Bias**





1. **Voltage Divider Bias**





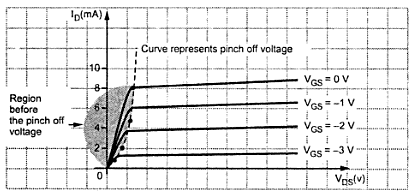


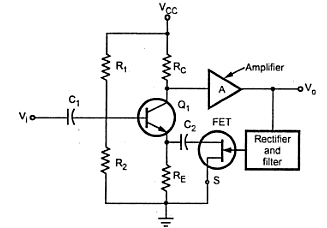




(Note : derivation everything same as biasing using transistor)

**10. Describe how a JFET can be used as a voltage variable resistor.(8)(May’07)(Nov’07)**

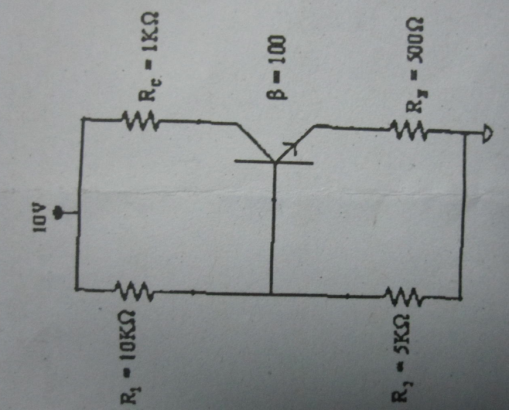
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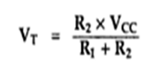
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* The region before the pinch off voltage, the drain characteristics is linear, here FET operation is linear.
* This region is useful as a voltage controlled resistor.
* FET is also referred to as a voltage-variable resister (VVR) or Voltage dependent resister(VDR)
* The voltage variable resistor property of FET can be used to vary the voltage gain of a multistage amplifier A as the signal level is increased. This action is called automatic gain control (AGC)
* Here maximum value of signal is taken , rectified and filtered to produce a DC voltage proportional to the output signal level. This voltage is applied to the gate if JFET, thus causing the AC resistance between the drain and source resistance.
* When the output signal level increases , the drain to source resistance also increase , increases the effect of RE Increase in RE cause the gain of transistor Q1 to decrease the output signal.
* Exactly reverse process takes place when output level decreases. Therefore the output signal level is maintained constant
* Q1 are not affected by JFET since FET is isolated from Q1 by means of capacitor C2.

**11. For the given circuit calculate VCE and IC where β = 100 for the silicon transistor**

**(May’12)**

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**VT  = 5K x 10V**

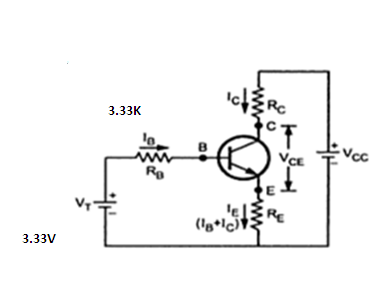
**5K + 10 K**

**VT  = 3.33V**

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**RB  = 3.33KΩ**

**Simplified equivalent diagram**

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**Apply KVL to the base circuit**

VT = IBRB+VBE+IERE

VT = IBRB+VBE+(1+β)IBRE

VT = IB[RB+(1+β)RE ] +VBE

= IB

IB =

**IB = 78.19µA**

Ic = β IB

**Ic = 7.819mA**

**Apply KVL to the output side**

VCC = ICRC+VCE+IERE

VCE = VCC – ICRC- IERE

VCE = VCC – ICRC- (1+β)IBRE

VCE = 10 – 7.819 mA 1 K - 101 x 78.19 µA x 0.3K

VCE = 2.1 V